



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,487	12/10/2003	Sung Bo Hwang	P69369US0	5410
136	7590	11/18/2004	EXAMINER	
JACOBSON HOLMAN PLLC 400 SEVENTH STREET N.W. SUITE 600 WASHINGTON, DC 20004			THOMAS, TONIAE M	
			ART UNIT	PAPER NUMBER
			2822	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/731,487

Applicant(s)

HWANG, SUNG BO

Examiner

Toniae M. Thomas

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau. (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>12/10/03</u> . | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This Office action is a first Office action on the merits of Application Serial No. 10/731,487. Currently, claims 1-5 are pending.

#### ***Specification***

2. The disclosure is objected to because of the following informalities: the term "ploy methyl metacrylate" should be "poly methyl metacrylate" (page 3, line 18 and page 6, line 4). Appropriate correction is required.

#### ***Claim Objections***

3. Claim 2 is objected to because of the following informalities: the term "ploy methyl metacrylate" should be "poly methyl metacrylate" (claim 2, line 1). Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. *Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US 6,365,506 B1) in view of Hawker et al. (US 6,107,357).<sup>1</sup>*

The Chang et al. patent (Chang) discloses a method of forming an insulating film in a semiconductor device (figs. 3A-3H and accompanying text).

---

<sup>1</sup> The Applicant submitted the Chang et al. patent as prior art.

The method comprises the steps of: forming a low dielectric constant (low-k) insulating film 23 on a semiconductor substrate in which various elements for forming the semiconductor device are formed (fig. 3A and col. 3, lines 32-36); and forming a dual damascene pattern in the low-k insulating film (figs. 3E-3H and col. 3, line 58 - col. 4, line 10). The low-k insulating film is a porous low-k insulating film (abstract, lines 11-14).

While Chang discloses that the low-k insulating film is porous, Chang lacks anticipation in not teaching that the porous low-k insulating film is formed by: forming a low-k insulating film containing a foaming agent on the substrate; and performing an annealing process so that the foaming agent reacts to form pores in the low-k insulating film.

The Hawker et al. patent (Hawker) discloses a method for forming a low-k insulating film in a semiconductor device (figs. 1-5 and col. 11, line 6 - col. 12, line 9), wherein the low-k insulating film is porous (abstract, lines 7-11 and col. 10, lines 51-54). The method comprises the steps of: forming a low-k insulating film 10 containing a foaming agent on a substrate 2 (col. 11, lines 27-39 and col. 10, lines 6-36); and performing an annealing process so that the foaming agent reacts to form pores in the low-k insulating film (col. 11, lines 39-41 and col. 10, lines 37-49).

In one embodiment, poly methyl metacrylate (PMMA) copolymer and a high polymer having an aliphatic core are used as the foaming agent (col. 8, lines 6-21), as recited in claim 2.

In one embodiment, methyl silsesquioxane (MSSQ) is used as a matrix of the low-k insulating film, as recited in claim 3 (col. 6, lines 38-51).

In one embodiment, the annealing process is performed at a temperature in the range of 200° C to 500° C, as recited in claim 5 (col. 13, lines 25-37).

Since Chang and Hawker are from the same field of endeavor, the purpose for which Hawker is relied upon would have been recognized in the pertinent reference of Chang by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, to modify Chang in view of Hawker by forming the porous low-k insulating film 23 disclosed in Chang using the method taught by Hawker, because the porous low-k insulating film formed therefrom has a dielectric constant of less than 2.5 at 25°C (Hawker - col. 10, lines 54-56). In addition, the porous low-k insulating film has closed cell pores less than 10nm in diameter and a void percentage in the range of 5% to 35%, resulting in enhanced mechanical toughness, crack resistance, and improved isotropic optical properties (Hawker - col. 10, lines 56-62). The low-k film also has a low thermal expansion coefficient at elevated temperatures, which helps to prevent cracking during thermal processing (Hawker - col. 10, lines 62-66). Furthermore, the low-k film has mechanical properties that enable it to be chemically/mechanically planarized to facilitate lithographic formation of

Art Unit: 2822

multiple circuit levels in multilevel integrated circuit devices (Hawker - col. 10, line 66 - col. 11, line 3).

5. *Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang in view of Hawker as applied to claim 1 above, and further in view of Joubert et al. (US 6,326,302 B1).*

Chang does not teach that the dual damascene pattern is formed at a temperature of -50 °C to room temperature. The Joubert et al. patent (Joubert) discloses a method for forming a damascene pattern in a low-k insulating film (col. 3, line 40 - col. 4, line 27). The dual damascene pattern is formed at room temperature using a plasma etching process (col. 3, lines 58-67).

Since Chang and Joubert are from the same field of endeavor, the purpose for which Joubert is relied upon would have been recognized in the pertinent art of Chang by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Chang and Hawker by forming the dual damascene pattern at room temperature, as taught by Joubert, because the discovery of optimum process parameters, such as temperature, time, etc., are well within ordinary skill in the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

Art Unit: 2822

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*MMJ*

14 November 2004



**Mary Wilczewski**  
**Primary Examiner**